A Hardware and Software Perspective of the Fifth Materials on the International Space Station Experiment (MISSE–5)

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Abstract

Conducting space experiments with small budgets is a fact of life for many design groups with low-visibility science programs. One major consequence is that specialized space grade electronic components are often too costly to incorporate into the design. Radiation mitigation now becomes more complex as a result of being restricted to the use of commercial off-the-shelf (COTS) parts. Unique hardware and software design techniques are required to succeed in producing a viable instrument suited for use in space. This paper highlights some of the design challenges and associated solutions encountered in the production of a highly capable, low cost space experiment package.

Introduction

The Forward Technology Solar Cell Experiment (FTSCE) is a space solar cell experiment built as part of the Fifth Materials on the International Space Station Experiment (MISSE-5). It represents a collaborative effort between NASA Glenn Research Center (GRC), the Naval Research Laboratory (NRL) and the U.S. Naval Academy (USNA). The purpose of this experiment is to place current and future solar cell technologies on orbit where they will be characterized and validated. This is in response to recent on orbit and ground test results which have raised concerns about the in space survivability of new solar cell technologies and about current ground test methodology (ref. 1). The various components of the FTSCE are assembled into the passive experiment container (PEC) which is a 2-ft by 2-ft by 4-in. folding metal container that will be attached to the outer structure of the international space station (ISS) by an astronaut. Test data is transmitted to Earth and stored in on-board back-up memory. At the end of a nominal one year mission, the PEC will be removed and returned to Earth. The experiment is designed to remain in orbit for two and a half years if the situation arises.

MISSE-5 Hardware Overview

MISSE-5 is placed in a PEC used to fly space environment samples to space and back (fig. 1). It is attached to the exterior of the ISS during an extravehicular activity (EVA) to expose samples to space. For MISSE5, these samples are 39 advanced technology solar cells positioned on the side of the PEC that faces the sun (fig. 2). The technologies include state-of-the-art and next generation multijunction InGaP/GaAs/Ge, heteroepitaxial GaAs/GeSi/Ge, and amorphous Si and $CuIn(Ga)Se_2$ thin film solar cells (ref. 2).
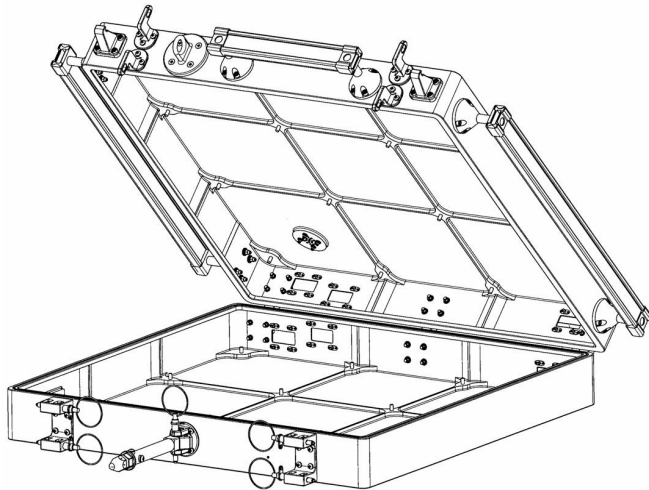
Figure 1.—This is a drawing of the 2-ft by 2-ft by 4-in. passive experiment container (PEC).
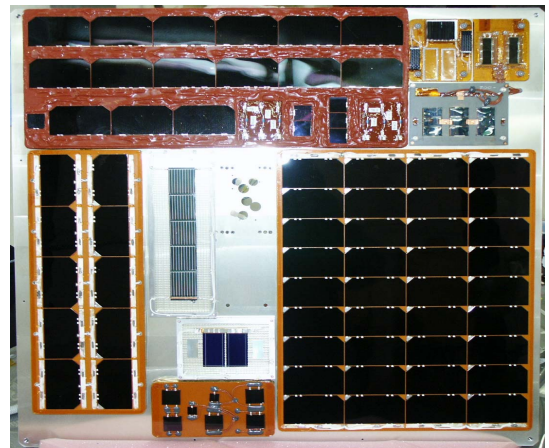

Figure 2.—This is a photograph of the FTSCE experiment deck to be placed into the MISSE5 PEC.

In addition to these cells are a number of other sensors to include two-element position sensitive diodes for sun position sensing, single point solar cells for radiance and sun position sensing and temperature sensors in the form of resistance temperature devices (RTD) and three terminal temperature sensors from Analog Devices (AD590). The electronics assembly to interrogate these sensors and to communicate with the second prototype communication satellite system (PCSAT2) has been provided by NASA GRC personnel. The PCSAT2 communication system will be used to telemeter test data to Earth and to telemeter command and control from earth to the NASA GRC electronics using the International Telecommunication Union (ITU) Amateur Satellite Service. In the event of a communications failure, the NASA GRC electronics will continue to operate in a stand alone mode, taking data according to time, temperature and sun position schedule. Data normally sent to earth
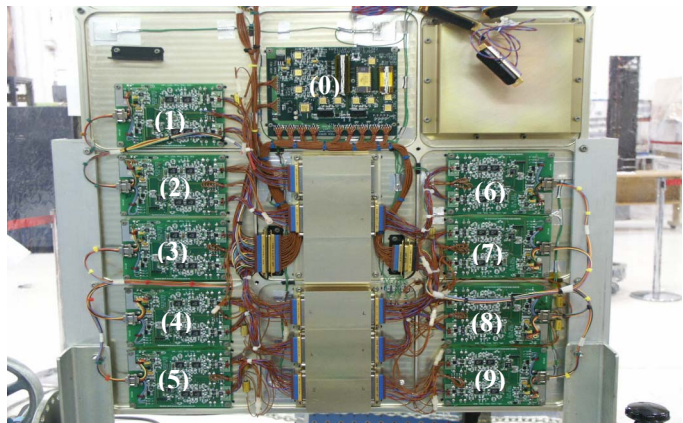

Figure 3.—This is a photograph of the data acquisition electronics designed, manufactured, programmed and tested by engineers and technicians at NASA Glenn Research Center mounted on the electronics deck. There is a single "main" microprocessor board (0) that controls nine "daughter" boards (1 to 9), which record the current-voltage (IV) curve, temperature, and sun angle data.

will also be archived in on-board flash memory. The PEC will be recovered in a year or two during a subsequent EVA and returned to earth where its data can be downloaded from the flash memory. The NASA GRC electronics are made up of the main microcontroller board , or "mother board" which is numbered board 0 and nine data acquisition boards "daughter boards" numbered 1 through 9 (fig. 3).

Mother Board Hardware

The mother board is centered about a core borrowed from the Mars array technology experiment (MATE) (ref. 3) and the dust accumulation and removal technology experiment (DART) (refs. 4 and 5). These experiment packages from the scrubbed Mars 2001 mission were designed, qualified and shipped to fly by the same NASA GRC personnel. This core is made up of an 80C32E radiation tolerant (rad-tolerant) microcontroller from Temic (now Atmel), a radiation hardened (rad-hard) 8Kx8, 67164 RAM from UTMC (now Aeroflex) and a rad-hard 32Kx8 28F256 EEPROM from SEi (now Maxwell). Supporting this core is 54AC glue logic from National which is single event latch-up (SEL) immune with a linear energy transfer (LET) greater than 120 and single event upset (SEU) immune with a LET in the range of 40 to 60 (refs. 6 and 7). The expected mission environmental specification is given at an LET of 37. Total dose is not an issue with shielding because radiation levels fall below 1 Krad-Si (1 rad-Si=100 ergs/grams of silicon) (refs. 8 and 9). The microcontroller is rad-tolerant such that it is latch-up hard to a LET greater than 120 but is SEU hard only up to a LET of 5. Testing at Temic showed that SEUs can occur in the 80C32E's RAM. Mitigation for this upset has been effected by placing all possible RAM operations, specifically microcontroller state information, in the hard external RAM, and by a triple modular redundant (TMR) power-up, brownout, watchdog-timer reset circuit (fig. 4). Thus, if the 80C32E gets lost, either internally or through SEUs in the glue logic, it will be reset and forced into a cleansing reboot. The 80C32E can endure a total dose exceeding 100 Krad-Si (ref. 10).
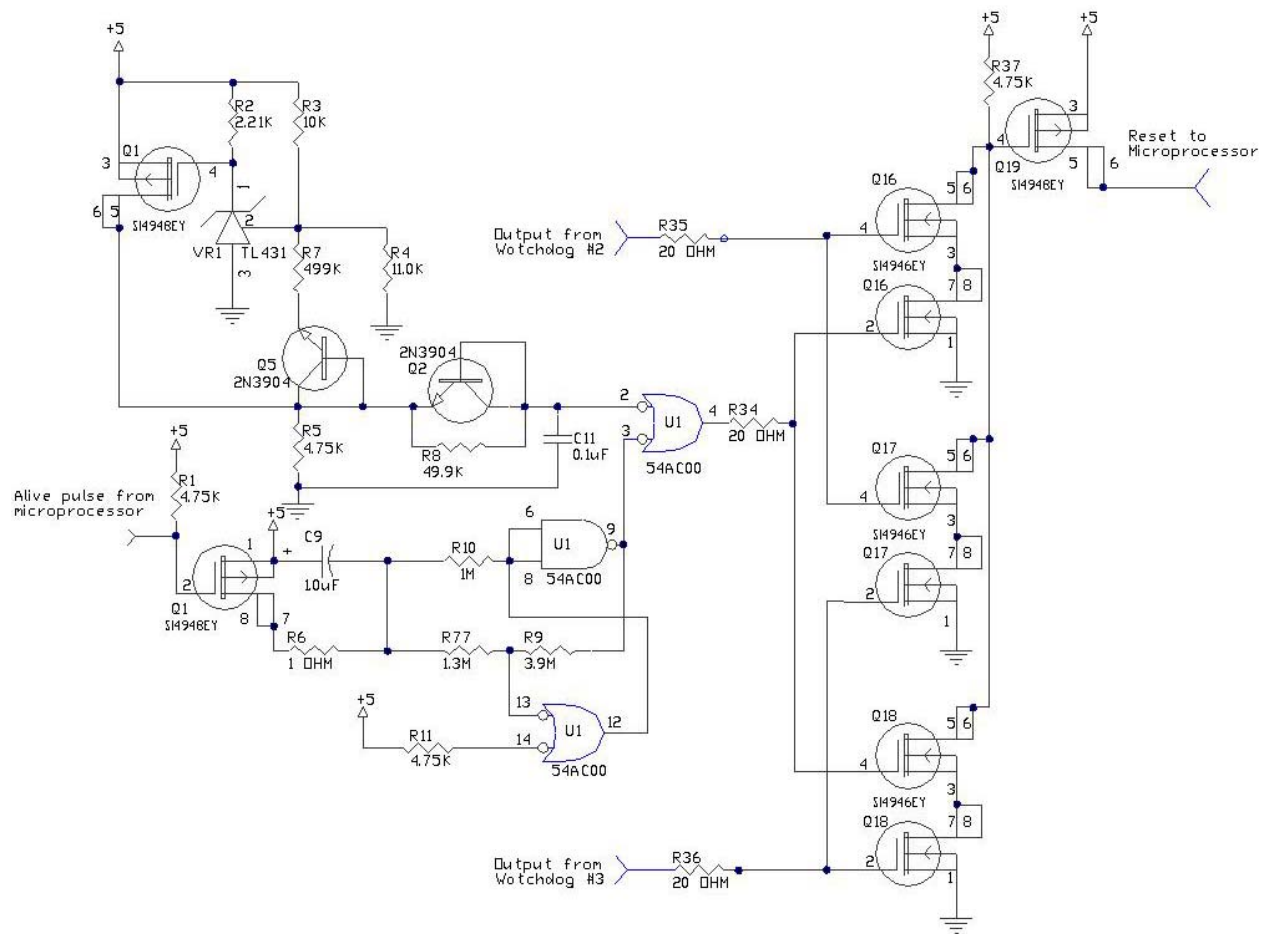

Figure 4.—Power-up, brownout, watchdog-timer reset circuit.

The 8Kx8, 67164 RAM from UTMC is rad-hard under specified operating conditions to endure a total dose of 1 Mrad-Si, to be free from latchup and to have a SEU rate of about 10^{-13} errors/ bit-day (ref. 11). Data is scratch padded in the RAM and the state of the microcontroller is stored there as mentioned earlier. As further brown out mitigation, we have experimentally shown that the device retains its contents down to Vdd = 2 volts indefinitely and also does so repeatedly for 37 mS excursions down to Vdd = 0.7 volts. Therefore, the 32Kx8 28F256 EEPROM from SEi is considered rad-hard for this mission. Its SEL and SEU thresholds exceed a LET of 120. It can also endure a total dose over 100 Krad-Si (ref. 12). It is only susceptible during write operations (SEU LET=20) but no writes shall be effected during flight. The 28F256 stores the program memory and data fields for the mission. Beyond the microcontroller core is the power-up, brownout, watchdog-timer reset circuit, the power switching for the daughter boards, the serial communications multiplexer and level translators for the daughter boards, the ground support equipment (GSE) and PCSAT2, the mother board power control and the twin flash memory banks.

Power control for the mother board is provided by a switched +16 volt (+12 nominal) bus. A parallel metal-oxide semiconductor field-effect transistor (MOSFET) switch is provided on the mother board which can be externally operated by PCSAT2 if ground operations feel that a wake-up call is necessary due to some detected anomaly. A low on this line removes power from the board for a sufficiently long period to destroy RAM contents and reset the microprocessor.

The power-up, brownout, watchdog-timer reset circuit is realized as three identical circuit slices joined to a voting circuit (fig. 4). At least two of the three slices have to be in temporal agreement that a reset must occur for one to be issued. At power-up, the microcontroller is held in reset for 100 milli-seconds after Vdd exceeds 4.75 volts. A TL431 in each slice functions as a comparator and modulates the reset pulse. A majority of slices must agree on a power-up reset for one to be issued. The same TL431 comparator circuits will issue a reset after Vdd recovers from a drop below 4.75 volts. This function is to keep the microcontroller from doing anything foolish (such as errant writes to RAM) while in a brown-out state. A majority of slices must agree on a brown-out reset for one to be issued. Each slice contains a watch-dog timeout function. The microcontroller must perform 10 sequential write operations to the memory address uniquely associated with each watch-dog during a 1.4 second period in order to prevent a timeout. If two or more watch-dogs timeout, a 1 second reset will be issued.

Power switching for the daughter boards is accomplished by a nine bit pattern. A tri-state shift register is loaded with a "0" in each location corresponding to a daughter board chosen for power-up. Thus, boards can be selectively switched on or off. To conserve power, and to reduce the probability of SEUs under bias, all daughter boards are naturally powered down. During operations any subset of boards may be powered up depending on the state of operations and on the state of daughter board health. For example, every ten minutes temperature data is taken. Only the boards possessing temperature sensors need to be powered up. Also, if the microcontroller notices that a board is flakey or non-operational, it can be masked off and permanently precluded from power up. The shift register is made up of a quad 2-input NAND gate (54AC00), an octal d-type flip-flop (54AC374) and an octal transceiver (54AC245). The daughter board power up signal line is pulled up to +16 volt (+12 volt nominal) and is diode protected. To power up the daughter board, this signal must be pulled to ground. Power switch signal level shifting is effected by a XP04311 dual NPN/PNP transistor array connected to each bit in the shift register and to its corresponding daughter board.

The twin flash memory banks are made up of two K9F3208W0A, 4Mx8 NAND flash memories. This is an "end-of-life" part from Samsung which was the result of a renaming of the KM29W3200. The KM29W3200 is the extended voltage (2.7 to 5) volt version of the KM29N32000. The KM29N32000 was radiation tested by Maxwell and found to be hard to a total dose of 4.45 KRAD biased and 21 Krad-Si unbiased and to have an SEL LET and SEU LET of > 60 (ref. 13). The K9F3208W0A is of the same process as the KM29N3200 and can operate at a lower voltage. Thus we cannot guarantee that they will operate the same as the KM29N3200 in a radiation environment, but we are comfortable enough to design it into the system redundantly with power down control and circuit isolation. Every fifteenth data set
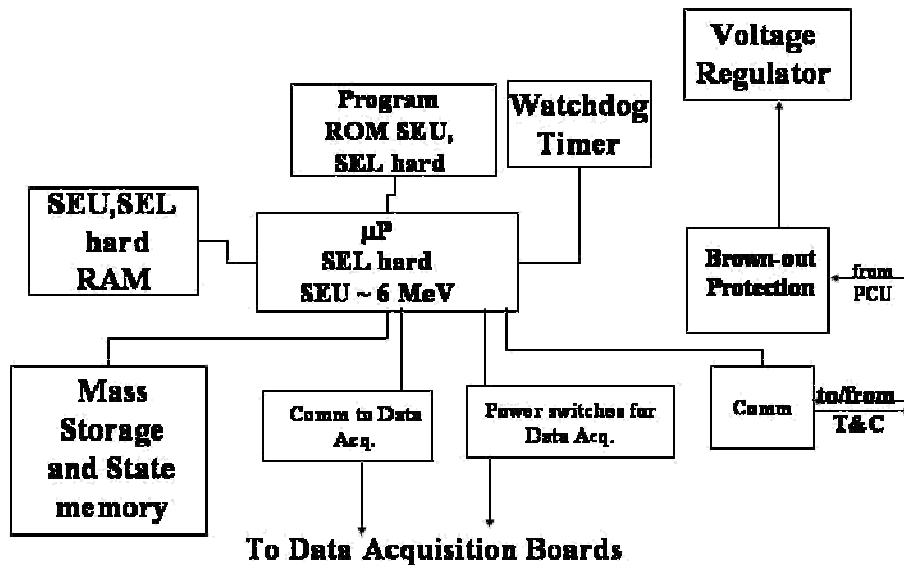
Figure 5.—Block diagram of mother board hardware.

acquired from the daughter boards is written to both flashes. It is only at this time, about once per day, that the flashes are under bias. Two are used as a redundant measure should any upsets occur during a write operation. The flash is capable of storing 2.4 years of mission data.

The serial communication multiplexer permits only one communication channel to be open at a time. A four bit pattern is written to two MUX16, JFET multiplexers; one for transmit and one for receive. The MUX16, using bipolar and JFET technology, is rad- hard for this application. Furthermore, the MUX16 requires a Vdd which is a minimum of 4 volts greater than the largest signal it will have to pass. Thus, it is powered by the switched +16 volt (+12 nominal) bus. The daughter boards use 3.3 volt CMOS levels for serial communication therefore transceivers are not used to link to the microcontroller. On the other hand, the GSE and PCSAT2 require 2VN3310 MOSFETS and 2N2222 transistor circuits to provide level translation for valid RS232 transmit and receive levels. The GSE and PCSAT2 are paralleled off of the same channel as there shall never be a case where both are attached to the system simultaneously. Thus, GSE operations can be carried out with mother board not knowing if it is GSE or PCSAT2 to which it is communicating. This allows us to use the same software for ground and flight activities. A block diagram of the mother board hardware is shown in figure 5.

Daughter Board Hardware

There are nine daughter boards. Each is capable of autonomously acquiring 32 point I-V curves from each of four separate solar cells. Each board can also support a two-element position sensitive diode for sun position sensing and a combination of single point solar cells for radiance and sun position sensing and temperature sensors in the form of RTDs and AD590s. The daughter board cored is a C8051F006 microcontroller by Cygnal, which is not a flight grade part. Conversations with an application engineer at Cygnal revealed that they have not been able to force the part into a full scale latch-up, but have been able to create local latch-ups at output pins if those pins were required to source or sink over 20 mA. No such occurrences were destructive to the part nor did they otherwise disrupt program execution. The local events could be corrected by removing current from the pin or from the part. With this in mind, care was taken to resistively protect each output such that there would never be a source or sink condition over 10 mA. A circuit based on an auto-reset electronic circuit breaker (LT1153) was designed to remove power

from the digital portion of the board if the quiescent current were to reach 100 mA or if a brown-out were detected. Power to each daughter board is controlled by a pull down circuit on the mother board. At power-up, a control line is pulled low by the mother board, causing a MOSFET switch on the daughter board to apply +3.3 volts to the microcontroller and +7.5 volts to the DG406 analog multiplexer and to the analog section consisting of primarily of LT1014ISW quad operational amplifiers (opamps). These amplifiers are bipolar amplifiers and are parametrically sound up to Krad-Si levels. During power down, a MOSFET circuit automatically switches a shunt resistor across each cell to keep it under constant load (fig. 6). Thus, during non-operation, each cell is still sourcing current. In the event that a board fails to be powered up for some reason, at a minimum, the cell will have been aged under load stress and purposeful post flight evaluation can be conducted. At power-up, the microcontroller must actively disable this function to allow for I-V curve generation.

A brown out detect circuit is connected to the LT1153 circuit to remove power to the microcontroller in the event that the +16 (+12 volt nominal) rail drops lower than +9.5 volts which is the lower limit for +7.5 volt analog power regulation (fig. 7). Also at power-up, the microcontroller does a self check to include RAM test and program memory checksum. The results of this test are queried by the mother board during the initiation of serial communications. If an error is detected, the mother board may, via ground command, mask it off from future power-up cycles, deeming it a very bad board.
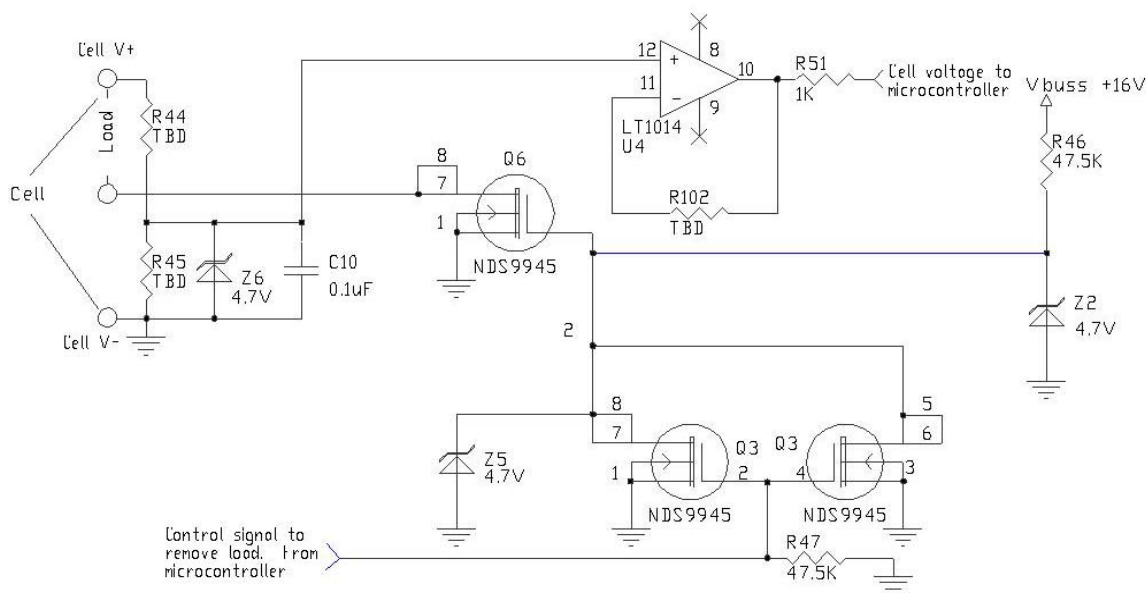

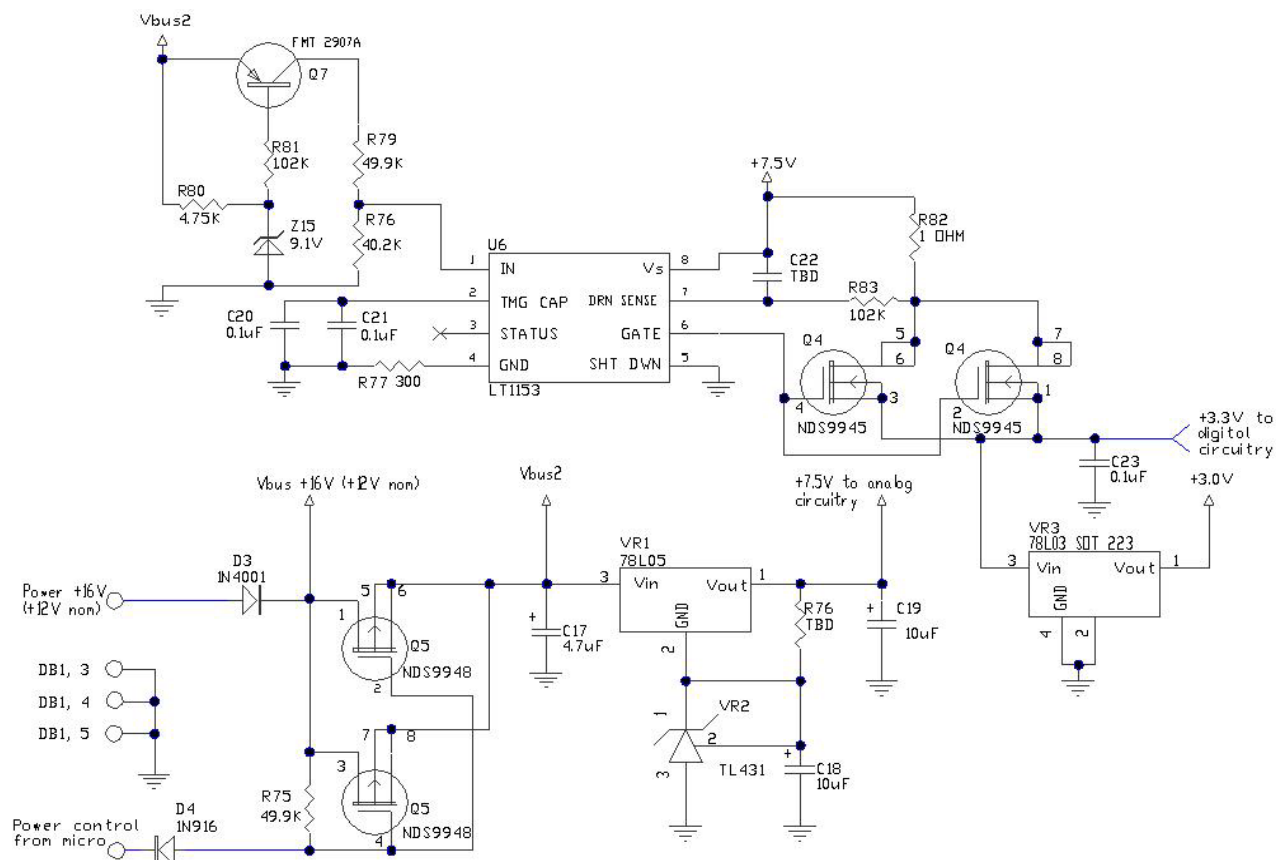Figure 6.—Cell load switch and voltage output.
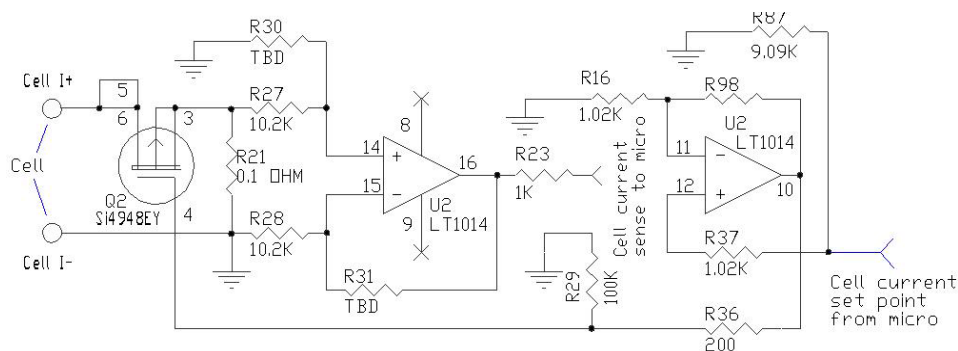
Figure 7.—Power monitor circuit.

Figure 8.—Variable cell load and current sense.

Each daughter board can perform a 32 point I-V curve on each of four separate solar cells. Unlike the I-V curve circuit in MATE, which used a current source to pump the cell, the circuit in the daughter board simply has a series MOSFET and low ohm sense resistor across the cell (fig. 8).

Digital to analog converter outputs from the microcontroller are amplified by an opamp circuit to provide bias to the MOSFET gate. A difference amplifier across the sense resistor provides a voltage analogous to the current sourced by the cell. The sense resistor is referenced to ground and is in the source circuit of the MOSFET. This provides negative feedback against self heating induced fluctuations in the channel resistance versus gate to source voltage function. A voltage divider/opamp buffer across each cell provides a voltage analogous to the voltage across the cell (fig. 6). While sweeping the digital to analog converter voltage, the microcontroller simultaneously performs analog to digital conversions (ADC) on

the current and voltage sense signals and creates the I-V curves. The gain and divider component values for the current sense circuits and the voltage sense circuits are chosen to reflect the short circuit current and the open circuit voltage of the cell on each channel. Resistor values are chosen to exploit the full ADC range of the microcontroller for each cell.

The microcontroller possesses only eight analog channels, but there are fourteen signals on the board that require observation. Therefore, a 1-of-16 analog multiplexer (DG406) is utilized to multiplex seven signals on one of the analog channels of the microcontroller thereby producing a total of fourteen analog channels. The DG406 was chosen because it will run on the single supply voltage of +7.5 volts and also because it is an epitaxial CMOS part which is expected to be latch-up resistant. If the LT1153 senses a current of draw over 100 mA, the microcontroller or the DG406 has presumably latched-up and power will be removed from the DG406.

A versatile two opamp circuit on the daughter board can be adapted to support two AD590 temperature sensors, two single point solar cells, one of each of the aforementioned or a single three wire measurement on an RTD (fig. 9). The inclusion, omission and/or component value choices determine the circuit function. Temperature measurements are important as they give a thermal profile against which the aging of the cells has occurred. Temperature measurements are taken every 50 seconds and stored every 10 minutes while I-V curves are taken approximately every 90 minutes or once per orbit. Single point solar cells are used for back-up sun position sensing and for radiometry.

Another two opamp circuit is included to condition the signals from a two element position sensitive photodiode (PSD) for sun position determination (fig. 10). The PSD elements are back biased by one diode drop to keep the device from forward biasing itself when high output currents drive its rather large series impedance. The opamps run in the transimpedance mode. A single forward biased diode shared by each amp's non-inverting input imposes a reverse bias at each inverting input's summing junction. The diode voltage is read by the microcontroller along with the IR value of the transimpedance amps. In this manner, the diode drop, now summed to the transimpedance values, can be subtracted from each signal by the microcontroller.
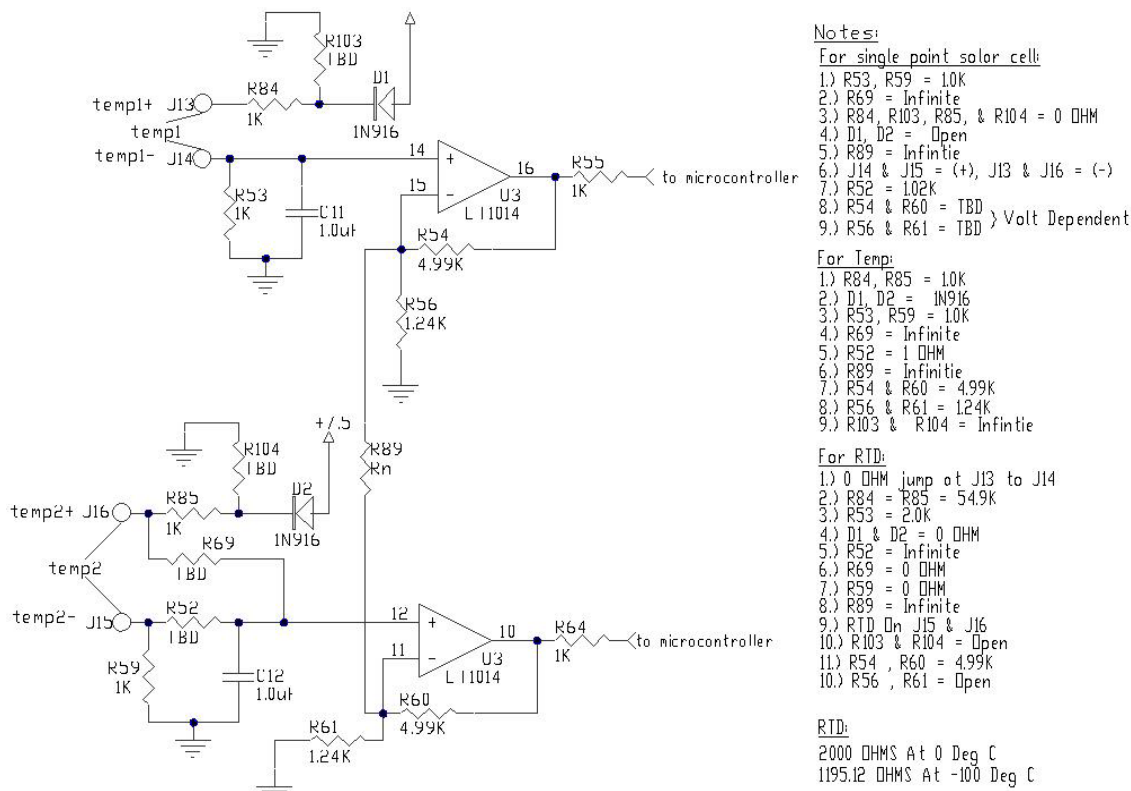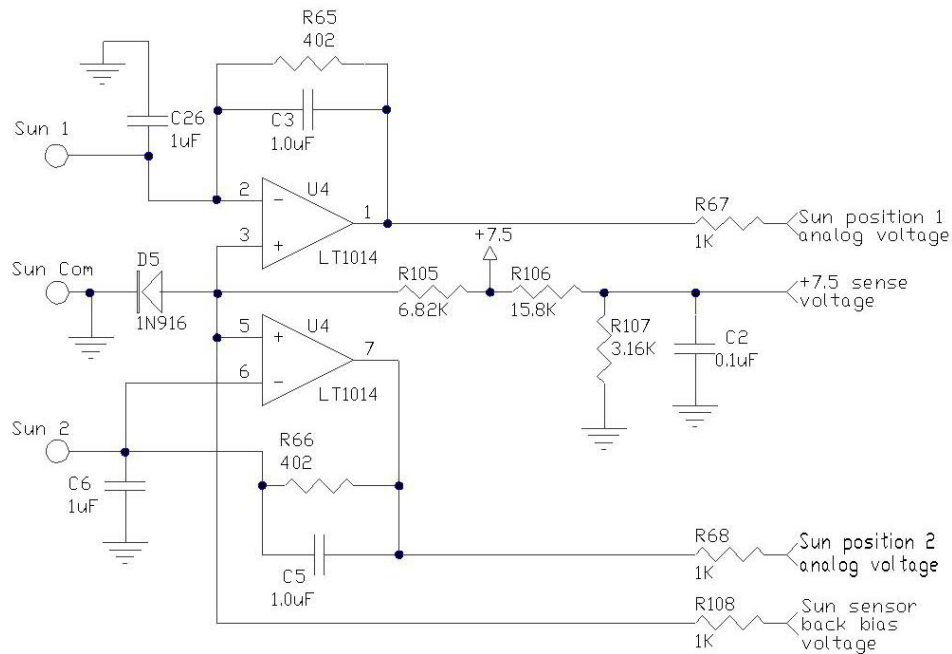

Figure 9.—Temperature circuit.

Figure 10.—Sun position sensor circuit.

Daughter Board Firmware

The daughter boards for MISSE-5 were designed to serve as multipurpose data acquisition units. Each board possesses eight sensor channels reserved for acquiring 32-point current-versus-voltage (IV) curves from four individual solar cells. Additionally, there are two sensor channels designed to support three different types of temperature sensor (AD590, Rtd, shorted cell). Lastly, four sensor channels are dedicated for reading sun position sensors. The multipurpose nature of these boards requires supporting software that allows for easy transition between many available sensor configurations. Consequently, the software is constructed with configuration blocks that define the on-board hardware, calibration scale factors and health check information for each of the nine flight boards and two laboratory boards. Any of these board setups is easily selectable and the information within the individual board configurations is readily available for customization.

The function of the main program is to query the serial port at a standard 9600 baud rate for commands sent by the mother board and perform the requested action. Its structure is illustrated by the flowchart in figure 11. All serial transfers start with a header byte of 0xFF and are terminated with a two byte cyclic redundant code (CRC). This simplifies the synchronization and validation of data packets sent to and from the daughter boards. The command and data block format is shown in figure 12. There are four commands recognized during the 30 millisecond window allotted for polling the serial port. The first command acquires temperature, sun position and health check data and stores it in memory. The second command acquires 32-point IV curves on each of four channels tied to a variety of solar cells and stores the information in memory. The third command requests the serial transfer of the temperature, sun position and health data. Finally, the forth command requests the serial transfer of all data stored in memory. An error message is transmitted if the program detects an errant command. Upon power-up, the program performs a RAM memory check and a ROM memory check. The temperature and sun sensor data are also acquired on power-up. If 70 milliseconds elapsed within the main program loop with no reset of the watchdog register, the microcontroller is reset and the program re-initialized.
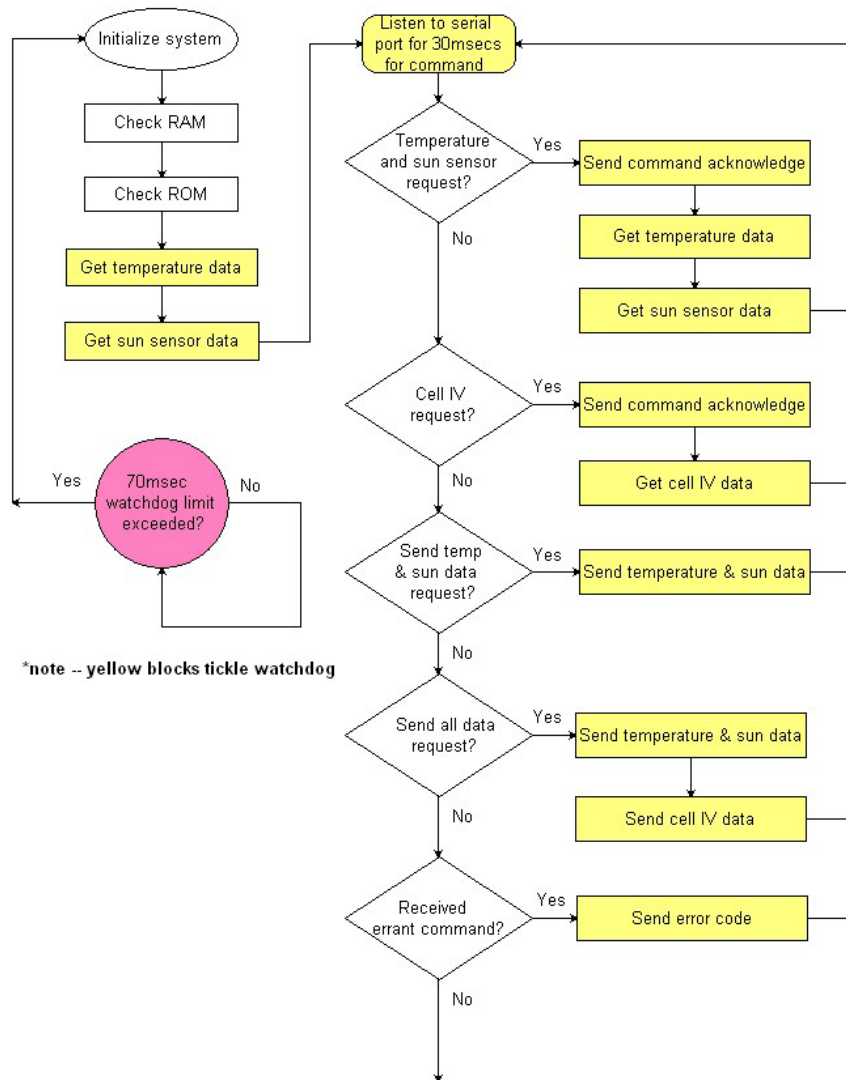
Figure 11.—Main program flowchart.

Command format

Byte #	Contents
1	Header = 0xFF
2	Command 1=get temp,sun,health data 2=get cell IV curves 3=send temp,sun,health data 4=send all data
3	Isc1 lo-byte (*see note1)
4	Isc1 hi-byte
5	Isc2 lo-byte (*see note1)
6	Isc2 hi-byte
7	Isc3 lo-byte (*see note1)
8	Isc3 hi-byte
9	Isc4 lo-byte (*see note1)
10	Isc4 hi-byte
11	CRC lo-byte
12	CRC hi-byte

*note1—(for Isc auto-calculate mode use 0x8000)

Data Format (Temperature, Sun Sensor and Health Data)

Byte #	Contents
1	Header = 0xFF
2	Temperature,Sun,Health ID = 0x01
3	Sun0 lo-byte
4	Sun0 hi-byte
5	Sun1 lo-byte
6	Sun1 hi-byte
7	Temperature1 lo-byte
8	Temperature1 hi-byte (*see note2)
9	Temperature2 lo-byte
10	Temperature2 hi-byte (*see note2)
11	Board Temperature lo-byte
12	Board Temperature hi-byte
13	Health Flag: Bit0=ROMFail (0=passed, 1=failed) Bit1=RAMFail (0=passed, 1=failed) Bit2=V1Timeout (0=passed, 1=timed out) Bit3=V2Timeout (0=passed, 1=timed out) Bit4=V3Timeout (0=passed, 1=timed out) Bit5=V4Timeout (0=passed, 1=timed out) Bit6-Bit7 (not used)
14	CRC lo-byte
15	CRC hi-byte

*note2 – (Bits 15 & 14 used to indicate temperature sensor type:
0x0000=AD590,0x4000=Rtd, 0x8000=Shorted Cell)

Data Format (Cell IV Data)

Byte #	Contents
1	Header = 0xFF
2	Cell IV ID=0x02
3	Cell1 Current @ Isc lo-byte
4	Cell1 Current @ Isc hi-byte
5	Cell1 Voltage @ Isc lo-byte
6	Cell1 Voltage @ Isc hi-byte (*see note3)
	↓↓↓↓
127	Cell1 Current @ Voc lo-byte
128	Cell1 Current @ Voc hi-byte
129	Cell1 Voltage @ Voc lo-byte
130	Cell1 Voltage @ Voc hi-byte (*see note3)
131	Cell2 Current @ Isc lo-byte
132	Cell2 Current @ Isc hi-byte
133	Cell2 Voltage @ Isc lo-byte
134	Cell2 Voltage @ Isc hi-byte (*see note3)
	↓↓↓↓
255	Cell2 Current @ Voc lo-byte
256	Cell2 Current @ Voc hi-byte
257	Cell2 Voltage @ Voc lo-byte
258	Cell2 Voltage @ Voc hi-byte (*see note3)
259	Cell3 Current @ Isc lo-byte
260	Cell3 Current @ Isc hi-byte
261	Cell3 Voltage @ Isc lo-byte
262	Cell3 Voltage @ Isc hi-byte (*see note3)
	↓↓↓↓
383	Cell3 Current @ Voc lo-byte
384	Cell3 Current @ Voc hi-byte
385	Cell3 Voltage @ Voc lo-byte
386	Cell3 Voltage @ Voc hi-byte (*see note3)
387	Cell4 Current @ Isc lo-byte
388	Cell4 Current @ Isc hi-byte
389	Cell4 Voltage @ Isc lo-byte
390	Cell4 Voltage @ Isc hi-byte (*see note3)
	↓↓↓↓
511	Cell4 Current @ Voc lo-byte
512	Cell4 Current @ Voc hi-byte
513	Cell4 Voltage @ Voc lo-byte
514	Cell4 Voltage @ Voc hi-byte (*see note3)
515	CRC lo-byte
516	CRC hi-byte

*note3 – (Cell voltage high-byte uses msb to indicate if acquisition of
IV point violated settling time limits. 0=passed, 1=timeout violation)

Acknowledge Command Request Format
(sent after unrecognized command received)

Byte#	Contents
1	Header = 0xFF
2	Acknowledge Command Request ID=0x03
3	CRC lo-byte
4	CRC hi-byte

Send Command Error Notification
(sent after all get data commands)

Byte#	Contents
1	Header = 0xFF
2	Send Command Error ID=0x04
3	CRC lo-byte
4	CRC hi-byte

Figure 12.—Command and data format.

After experimenting with the n-channel FET serving as a variable resistance load for IV tests performed on solar cells, some anomalies and non-linearities were discovered. Firstly, the rapid change in the FET junction temperature while transitioning through the short-circuit current (Isc) and max-power point portions of the IV curve causes channel resistance fluctuations within the FET (ref. 14). Consequently, the data points acquired in these regions of the IV curve are spurious. Furthermore, the relationship between the FET gate voltage and the channel resistance in non-linear. Fortunately, these issues can be resolved with some software mitigation illustrated by the flowchart in figure 13. Initially, all of the solar cells are continuously held under load with a fixed resistor that can be switched in or out of the circuit. The experiment begins by unloading the cell being tested and driving the FET completely off thereby floating the cells. After waiting 50 milliseconds for the drive circuitry to settle, a current reading (Ioffset) is taken to record the offset value that must be removed from all subsequent current readings. This presumes that the major contribution of the current at this load point is from offsets in the signal amplifier stages and not from the cell current through the open FET channel. Next, the FET is driven to
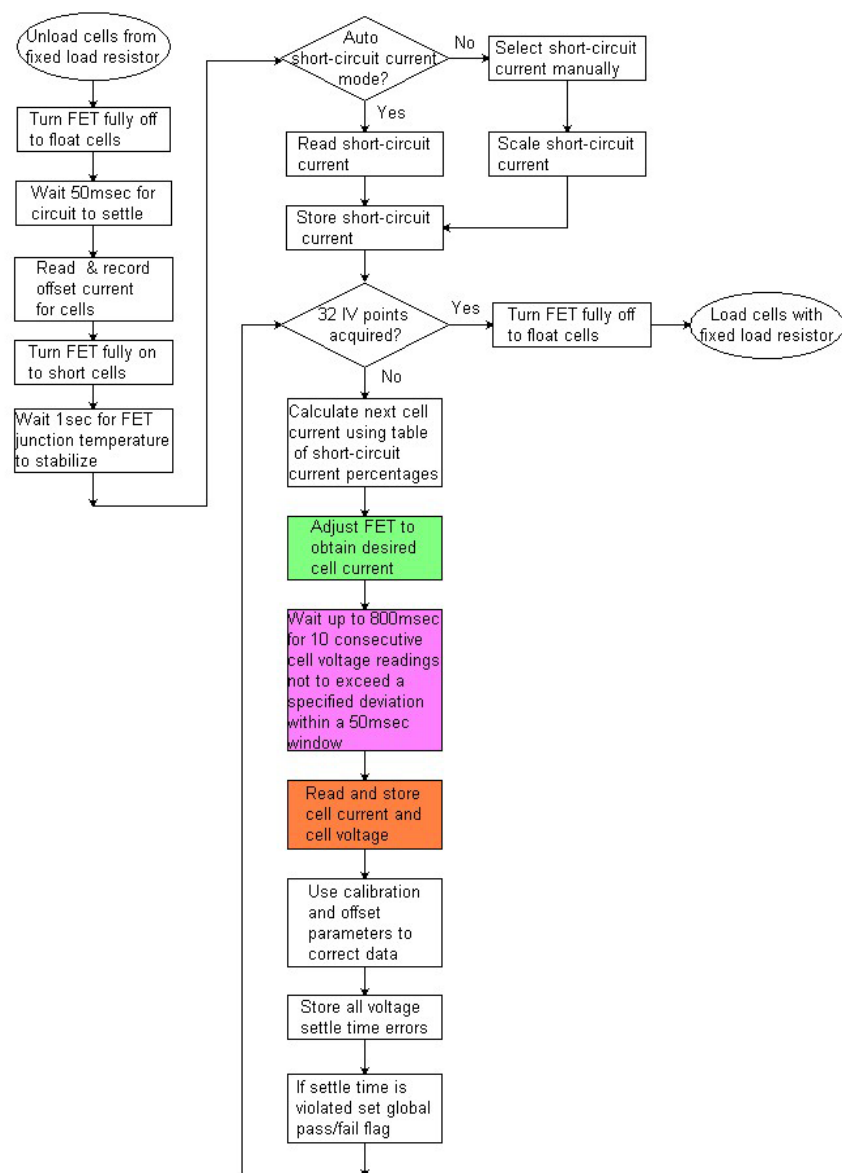

Figure 13.—Solar cell IV acquisition flowchart.

the completely on state thereby shorting the solar cell. As mentioned earlier, it was discovered that Isc causes heating within the FET which in turn alters the on resistance. If the FET junction temperature was not allowed to reach equilibrium before acquiring data, improper current readings were obtained. However, if an adequate waiting period for temperature stabilization was afforded (between 500 and 900 milliseconds), accurate, repeatable current readings were obtained. This program allows a full second before proceeding with current readings. Another assumption is that the FET has enough thermal mass to allow for the readings past the max power point to occur before junction cooling effects impact the data. After shorting the cell, either Isc is read or a value is manually entered and stored in memory. All subsequent points on the IV curve are driven by a table in ROM that selects the desired current points as a percentage of Isc. These values are sent to an algorithm that utilizes an onboard 12-bit DAC to drive the gate of the FET, through some buffer circuitry, such that the FET channel resistance produces cell currents as close as resolvable to the desired values. This procedure is illustrated by the flowchart in figure 14. With each change in cell current, the cell voltage is monitored ten times within a 50 millisecond time

Figure 14.—DAC control flowchart.

block. If the deviation within these ten samples is acceptable, the data point is considered stable and the current/voltage data pair is recorded in memory. On the other hand, if the voltage deviation is out of the specified range, another data point is taken 5 milliseconds later and the oldest data point within the ten point sample is discarded. A new deviation is then calculated and the process repeated. If after 800 milliseconds an acceptable deviation within the window of ten data points is not attained, the most recent current/voltage data pair is recorded in memory and flagged as unstable. This process is illustrated by the flowchart in figure 15.

Each acquisition that results in data stored to memory is actually the mean of twenty readings taken at 1 microsecond intervals. This procedure is illustrated by the flowchart in figure 16. After 32 current/voltage pairs have been acquired, the FET is turned fully off and the fixed load resister is reactivated. All data, with the exception of the temperature data, is output as a calibrated 12-bit ADC value that requires the proper scale factor and reference voltage to determine the actual sensor output. This also includes the current values sent to manually request a specific I_{sc} which must be converted from amperes to a 12-bit ADC value based on a current scale factor and the voltage reference. These scale factors, as shown in table 1, encompass the gains from the signal conditioning circuitry on the board and within the microcontroller. In contrast, the temperature output is always oK x10 with the two most significant bits used to indicate the type of temperature sensor (fig. 12).

TABLE 1.—CONVERSION FACTORS
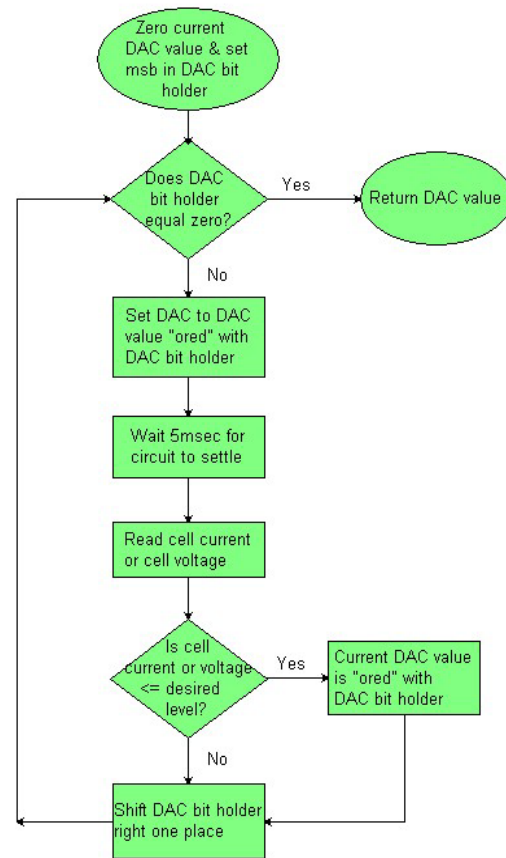
Board no.	V_{REF}	$V_{SCALEcell}$	$I_{SCALEcell}$	Temp1 Type T_{SCALE1}	Temp2 Type T_{SCALE2}	Sun Sensor
1	2.457	0.606	3.843	AD590 10.0	AD590 10.0	--------
2	2.424	0.606	3.843	AD590 10.0	AD590 10.0	--------
3	2.475	0.606	$3.941_{cell1-3}$, 3.843_{cell4}	AD590 10.0	AD590 10.0	--------
4	2.417	0.606	3.941	RTD 10.0	--------	--------
5	2.433	0.606	3.941	AD590 10.0	AD590 10.0	--------
6	2.441	0.606_{cell1}, 0.667_{cell2}, 0.333_{cell3}, 0.312_{cell4}	$3.843_{cell1-2}$, 19.71_{cell3}, 166.65_{cell4}	RTD 10.0	--------	SUN1,SUN2
7	2.435	0.99	13.43	GaAs/Si - Isc 27.7	AD590 10.0	SUN1,SUN2
8	2.439	0.623	25.5	Si – Isc 25.9	Si – Isc 25.9	--------
9	2.425	0.606	3.843	GaAs/Si - Isc 27.7	AD590 10.0	--------

$V_{CELL} = (V_{REF} * ADC_{CELL})/(V_{SCALEcell} * 4096)$ $I_{CELL} = (V_{REF} * ADC_{CELL})/(I_{SCALEcell} * 4096)$ $ADC_{SCcell} = I_{SCcell} * I_{SCALEcell} * 4096/$
$Temp_{AD590,RTD}$ (ºK) $= (V_{REF} * ADC_{TEMP})/(10 * 4096)$ $I_{GaAs/Si,Si}$ (mA) $= (V_{REF} * ADC_{SCcell})/(T_{SCALE1,2} * 4096)$
Θsunangle $= \tan^{-1}[\tan(64^o)*(SUN1-SUN2)/(SUN1+SUN2)]$;   SUN1,SUN2 $= ADC_{SUN1,2}$
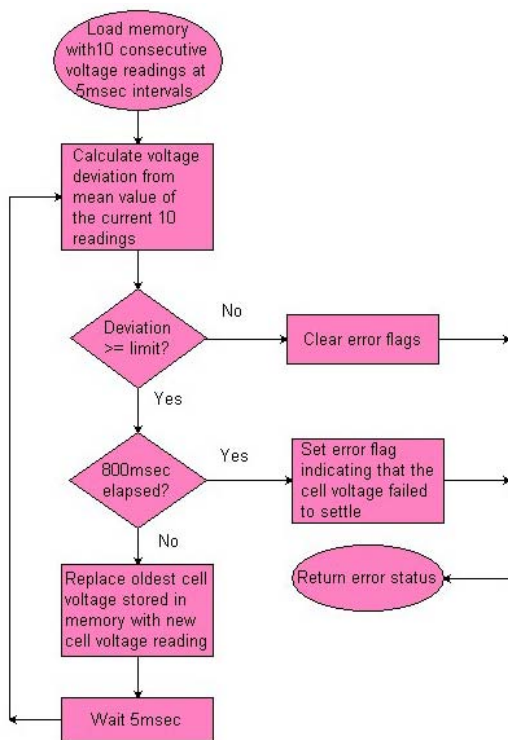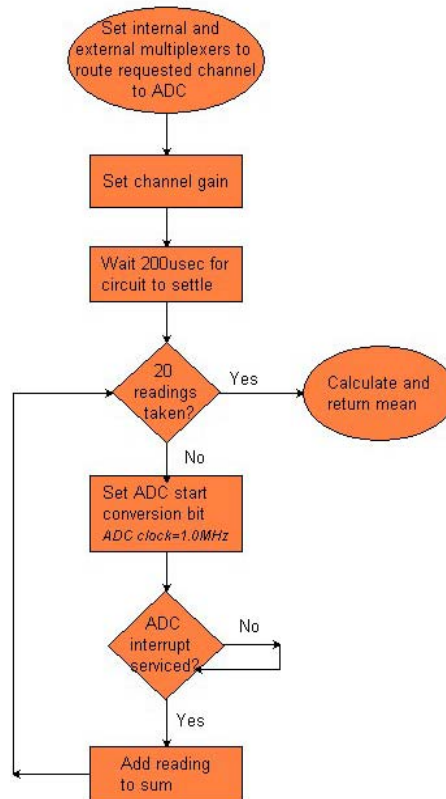

Figure 15.—Cell stabilization flowchart.

Figure 16.—Analog conversion flowchart.

The daughter boards have limited ability to detect total dose radiation damage and single event upsets "SEU." The initial random access memory "RAM" and read-only memory "ROM" tests check for permanently damaged memory cells which can be an indicator of total dose effects. These tests also check for transient bit flips which could be an indicator of a SEU. During serial data transfers, the CRC allows

for the detection and correction of single bit errors which again might indicate a SEU. If any of the nine daughter boards continuously fail the RAM and ROM tests after a cold start, it is considered unfit for service. The mother board can then remove the suspect board from the task queue.

Mother Board Firmware

The software is designed to autonomously take data when user defined conditions of sun angle and temperature are met. Also, the experiment can be commanded to measure on demand. Also, each daughter board can be commanded individually with a specific set of measurement criteria. This grants the scientists on the ground flexibility in customizing experimental data sets. For example, the daughter boards can be commanded to measure data once the sun angle is below a set threshold, which allows IV data versus angle of incidence data to be generated. Alternatively, the daughter boards can be commanded to measure once the temperature has exceeded a set threshold value, which allows IV data versus temperature to be generated. The software resident on the main microprocessor board is responsible for receiving commands from the terminal node controller (TNC) of PCSat2, decoding the commands, and passing the appropriate commands to the daughter boards. The main microprocessor software must also take the data from the nine daughter boards, translate it into printable ASCII characters and pass it to the TNC for down-linking by PCSat2. The main microprocessor software must also "oversee" the autonomous operation of the experiment, which consists of periodically recording readings from all of the temperature sensors to give a temperature profile for the PEC during each orbit and monitoring the temperature and sun angle data and determining if the measurement conditions have been reached. A flowchart illustrating the motherboard operations is shown in figure 17.
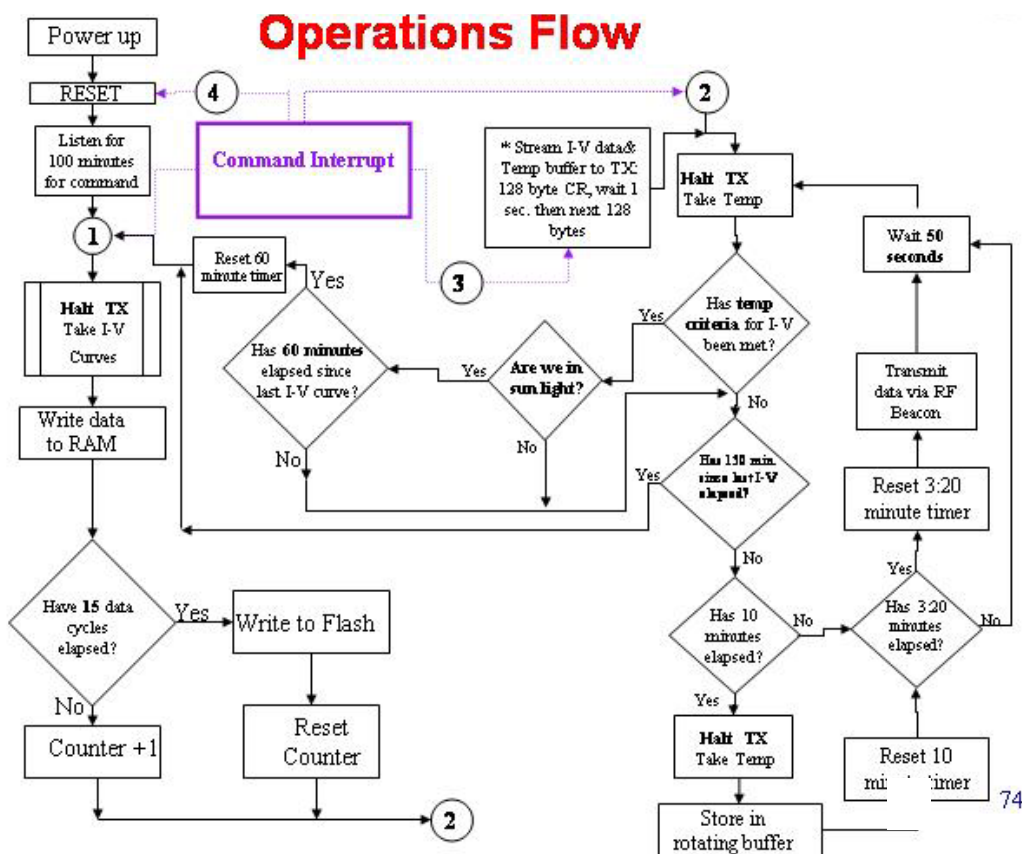

Figure 17.—Mother board operations flowchart.

The command structure used to control mother board operations consists of a sequence of 46 bytes illustrated in table 2.

TABLE 2.—LIST OF COMMAND VARIABLES

Command Byte #	Description					Default value
1-4	*Time*					All zeros
5						11000000
	SetTime	*Action*	*UseRelTemp*	*UseSun*	*UseRelSun*	
	7	6,5,4	3,2	1	0	
6	*SunThreshold*					01010000
7	*TempThreshold*					01110111
8-43	$I_{SC}Setpoint$					All zeros
44, 45	*DaughterEnable* (9 bits uses 2 bytes)					11111111, 00000001
46						0101XXXX
	TempID			*CRC*		
	7,6,5,4			3,2,1,0		

The motherboard clock value can be updated using the 4-byte value, *Time* and setting the bit *SetTime* to 1. If *SetTime* is set to 0, then the clock is not updated. There are eight command actions that can be uploaded to the motherboard. They are part of the command parameter *Action*, 3-bits, which is decoded in table 3.

TABLE 3.—ACTION PARAMETER DECODING

Action value	Mother board operation
000	Continue
001	Take I-V curves
010	Start Experiment
011	Transmit last data set
100	RESET motherboard
101	Send back current time
110	Write current data set to Flash
111	Transmit last data set stored in Flash

There are three criteria that have to be met in order to take an I-V curve. These criteria have been named Time-to-take-data, Sun Angle and Temperature. Below is a brief description of how the decision for each of these criterions is made.

Time-to-take-data: The goal is to take I-V curves once an orbit, and to provide a failsafe means for acquiring data in case of temperature or sun angle failure. I-V curves can be taken only after 60 minutes has elapsed since the last I-V curves and I-V curves will be taken if 150 minutes has elapsed since the last I-V curves. There are no command parameters associated with this decision.

Sun Angle: The sun angle is defined as the angle formed by the sun and the plane of the MISSE-5 solar cells. It is calculated from the two orthogonal sun sensors located in the same plane as the MISSE 5 solar cells. Valid sun sensor data is indicated by the output signals of the four shorted solar cells on MISSE-5 (daughter board 6, bytes 7 and 8; daughter board 7, bytes 7 and 8; daughter board 7 bytes 9 and

10; daughter board 8, bytes 7 and 8) exceeding a threshold value of 157. If any two of the four Isc cells are above this value, the sun sensor data is valid.

There are two ways the Sun Angle criterion can be met. Firstly, the sun angle is calculated to be equal to or less than *SunThreshold*, a one byte value corresponding to 0° to 64° in 0.25° increments. In this case, *UseRelSun* equals 0. Secondly, the sun angle is calculated to be equal to or less than the lowest sun angle value in the rotating buffer plus an offset of *SunThreshold* which varies from –32° to +32° in 0.25° increments. In this case *UseRelSun* equals 1. There is also a need to recover from a known sun sensor failure. *UseSun* is a 2-bit value that decodes as shown in table 4.

TABLE 4.—*USESUN* VALUE DEFINITIONS

UseSun value	Mother board operation
00	Use both sun sensors to calculate sun angle
01	Use only sun sensor "0" in sun angle calculation (Dac board 5 sun sensor; bytes 3 and 4, and 5 and 6)
10	Use only sun sensor "1" in sun angle calculation (Dac board 6 sun sensor; bytes 3 and 4, and 5 and 6)
11	Ignore sun angle when deciding to take I-V curves

Temperature: Here we pick a temperature to define when to take I-V curves. To make this decision we must first pick a temperature sensor. This choice of sensor is given in the command parameter *TempID* which is defined in table 5.

TABLE 5.—*TEMPID* VALUE DEFINITIONS

TempID value	Daughter Board	TempSensor*	Location
0000	1	1	Emcore AD590 panel Temp. "c"
0001	1	2	GaAs/Si AD590 panel Temp. "d"
0010	2	1	a:Si-SS AD590 temp "f"
0011	2	2	EMR Power panel AD590 temp "i"
0100	3	1	CIS AD590 Temp. "e"
0101	3	2	SPL panel AD590 temp "a"
0110	4	1	Emcore Temp RTD "K"
0111	5	1	Silicone AD590 Temp "h"
1000	5	2	SPL panel AD590 Temp. "b"
1010	6	1	SPL Temp RTD"J"
1011	7	2	Exp. Deck AD590 Temp. "m"
1100	9	2	a:Si kapton AD590 Temp. "g "
1101	5	Board Temp.	Daughter board 5 data bytes 11 and 12
1110	3	Board Temp.	Daughter board 3 data bytes 11 and 12
1111	Ignore temperature when deciding to take I-V curves		

* 1= bytes 7(lo) and 8(hi) in the daughter board data format and 2= bytes 9 and 10.

There are two ways to use the chosen sensor for the decision. Firstly, the temperature criterion is met when the sensor temperature is equal to or greater than the *TempThreshold* value. *TempThreshold* is a one byte value corresponding to 173.15 to 428.15 K, in one degree increments. In this case, the *UseRelTemp* bit equals 0. Secondly, the temperature criterion is met when the temperature is equal to or greater than the highest value of the sensor from the stored values in the rotating temperature buffer plus an offset

value of *TempThreshold*. In this case, *TempThreshold* is a one byte value corresponding to an offset of –225 to +40 in one degree increments. In this case, the *UseRelTemp* bit equals 1.

The variable *DaughterEnable* (9 bits) is used to power-on or power-off a given daughter board during the experiment. This is used in case a dangerous fault develops when powering on a particular daughter board. By setting this parameter low, a daughter board will never be turned on until a new command is sent to undo this action. It is a 9-bit parameter. The lsb corresponds to daughter board 1, if the bit is set high then the daughter board will be enabled during all measurement cycles. If the bit is set low, then it will remain off forever. The msb corresponds to daughter board 9. For example value of 111111111 means all boards are enabled during measurements, the value 000000000 means all boards are off, the value 0001100111 means only daughter Boards; 1, 2, 3, 6 and 7 are enabled.

The variable *IscSetpoint* (36-bytes) contains the starting Isc values or to use the auto Isc function. If all bits are low then auto Isc should be initiated (default mode). Each byte corresponds to the most significant 8-bits of a 12-bit starting Isc value. The least significant 4-bits should be set to 0000. The mapping of the 36-bytes is shown in figure 18.

LSB = daughter board 1, Cell 1
2nd byte = daughter board 1, Cell 2
3rd byte = daughter board 1, Cell 3
4th byte = daughter board 1, Cell 4
5th byte = daughter board 2, Cell 1
.
.
.
MSB = daughter board 9, Cell 4

Figure 18.—$I_{SC}Setpoint$ data format.

Discussion

In order to participate in a variety of small-budget space missions, engineers and scientist must learn to intelligently incorporate COTS parts into their designs. For MISSE5 a combination of rad-hard, rad-tolerant and latch-up immune parts were configured using TMR, current monitoring, watchdog-timer resets, data backup, error detection and recovery techniques in order to achieve the required level of radiation mitigation. The radiation performance of the COTS parts used in MISSE5 were guaranteed by design, process, testing or various combinations of the aforementioned. Software methods such as redundant data storage, RAM/ROM CRC checking, data packetization with CRC checking, timer watchdogs and repetitive measurements also serve as excellent tools to handle SEU and total dose effects on hardware. Lastly, there is no substitute for ingenuity as evidenced by the novel circuitry used to interrogate the solar cells. The traditional approaches would have either violated our weight budget with a multitude of load resistors or potentially damaged the cells by driving currents above Isc through the cell junctions. With all of the constraints of a space grade payload added to the constraint of a "coach" budget, we succeeded in producing an instrument that rivals laboratory grade equipment. Illustrating this point, a comparison of data measured by one of the daughter boards on a 3J InGaP/GaAs/Ge solar cell under illumination by the X-25 solar simulator in the NRL Solar Cell Characterization Laboratory with data measured by laboratory equipment under illumination by the same simulator is shown in figure 19 (ref. 2). This graph shows accurate reproduction of the IV curves obtained from calibrated laboratory equipment and the flight hardware. Furthermore, the deviation between data sets is at worst the same and in many regions of the IV curve smaller when using the GRC MISSE5 board when compared to the laboratory equipment.
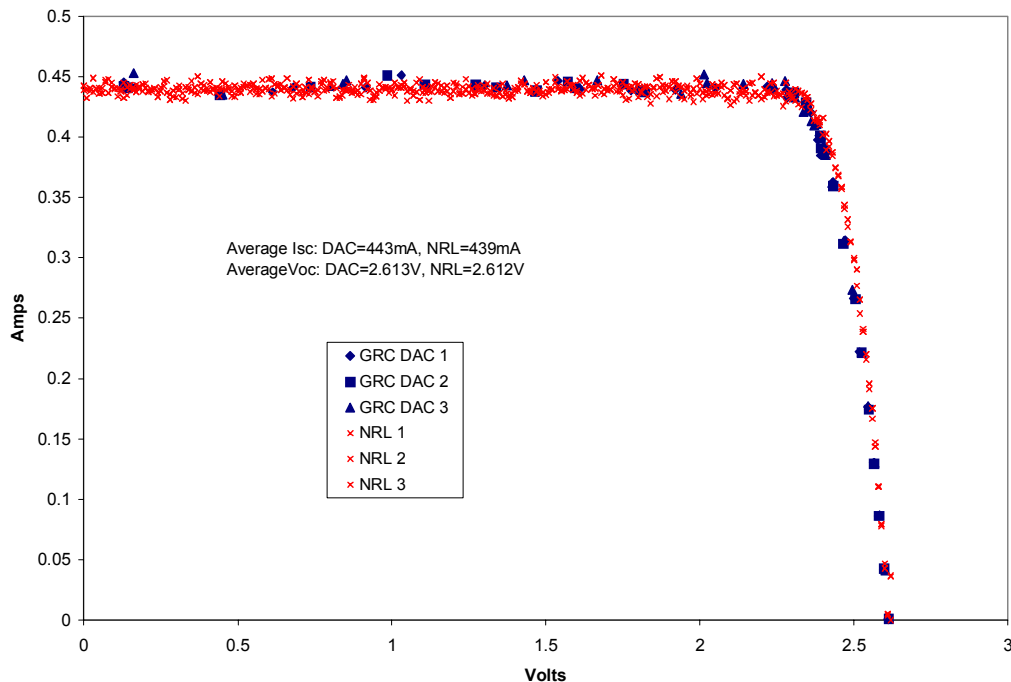
Figure 19.—This graph compares IV data measured on one of the InGaP/GaAs/Ge solar cells by a flight daughter (DAC) board and flight software compared to data measured on the same cell by laboratory equipment. In each case, three data sets were measured in succession, and the three curves are shown. All measurements were made under the same X-25 solar simulator in the NRL Solar Cell Characterization Laboratory.

Conclusion

The combination of process tracking COTS parts for radiation hard/tolerant pedigree and designing hardware and software with radiation mitigation in mind produced a reliable, space-worthy experiment package that also met our budget restrictions. Furthermore, most solar cell experiments employ a bank of switched load resistors or a programmable, bipolar current source for making the IV measurements. The MISSE5 MOSFET configuration is much lighter and smaller than the aforementioned and, as compared to the current source configuration, also safer for the cells, and thus signifies a substantial improvement in the state of the art. Lastly, data accuracy was not sacrificed by meeting our radiation and budget constraints. The MISSE5 equipment performed as well or better that the laboratory equipment used to verify its operation.

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13. ABSTRACT (Maximum 200 words)

Conducting space experiments with small budgets is a fact of life for many design groups with low-visibility science programs. One major consequence is that specialized space grade electronic components are often too costly to incorporate into the design. Radiation mitigation now becomes more complex as a result of being restricted to the use of commercial off-the-shelf (COTS) parts. Unique hardware and software design techniques are required to succeed in producing a viable instrument suited for use in space. This paper highlights some of the design challenges and associated solutions encountered in the production of a highly capable, low cost space experiment package.

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